IN THE CLAIMS

1 – 19 (canceled)

20. (currently amended) A method for reading a memory device comprising a dynamic ~~read only memory capacitor~~ random access memory coupled to first source/drain region of a non-volatile, nitride read only memory transistor, the transistor having a control gate coupled to a word line and a second source/drain region coupled to a bit line, the method comprising:

determining if the memory device is being accessed as a dynamic ~~read only~~ random access memory or as a non-volatile memory in response to a voltage level applied to the word line; and

if the memory device is accessed as a non-volatile memory, determining a current difference through the transistor to determine a state of the transistor.

21. (original) The method of claim 20 wherein a sense amplifier coupled to the bit line is used to determine the current difference by measuring differences in response time that changes in response to differences in a threshold voltage of the transistor.

22. (currently amended) A method for reading a memory device comprising a dynamic ~~read only~~ random access memory capacitor coupled to first source/drain region of a non-volatile, nitride read only memory transistor, the transistor having a control gate coupled to a word line and a second source/drain region coupled to a bit line that is coupled to a sense amplifier, the method comprising:

determining if the memory device is being accessed as a dynamic ~~read only~~ random access memory or as a non-volatile memory in response to a voltage level applied to the word line;

if the memory device is accessed as a non-volatile memory, charging the capacitor; and

determining a charge state of the transistor by measuring a plurality of currents supplied by the transistor through the bit line, each at a different gate voltage, and determining a response time of the sense amplifier at each gate voltage.

23. (currently amended) The method of claim 22 and further including reading the capacitor in response to the determination that the memory is being accessed as a dynamic ~~read only~~ random access memory.

24. (new) An electronic system comprising

a processor that generates control signals; and

a memory device coupled to the processor and operating in response to the control signals, the device comprising:

a memory array having a plurality of flash memory cells with integrated DRAM, each memory cell comprising a dynamic random access memory capacitor that provides a dynamic mode of operation and a nitride read only memory (NROM) transistor that provides a repressed non-volatile random access memory mode of operation, the NROM transistor coupled between the capacitor and a data line and acting as a transfer gate for the capacitor, the transistor comprising a control gate and a data storage layer; and

control circuitry that is adapted to execute a read operation of the memory array, the read operation comprises determining if the memory device is being accessed as a dynamic random access memory or as a non-volatile memory in response to a voltage level applied to the word line and, if the memory device is accessed as a non-volatile memory, determining a current difference through the transistor to determine a state of the transistor.

25. (new) The method of claim 24 wherein the NROM transistor is used as a shadow memory for the dynamic random access memory capacitor such that data from the capacitor is written to the NROM transistor upon a power-down condition of the system.

26. (new) The system of claim 24 and further including a sense amplifier coupled to the data line such that the sense amplifier can

27. (new) The system of claim 24 wherein data is written into the capacitor when the control gate is biased at a first potential and data is written into the transistor's data storage layer when the control gate is biased at a second potential that is higher than the first potential.

28. (new) A memory device comprising:

a memory array comprising a plurality of flash memory cells with integrated DRAM, each memory cell comprising a dynamic random access memory capacitor that provides a dynamic mode of operation and a nitride read only memory (NROM) transistor that provides a repressed non-volatile random access memory mode of operation, the NROM transistor coupled between the capacitor and a data line and acting as a transfer gate for the capacitor; and

control circuitry coupled to the memory array and adapted to execute a read operation of each memory cell, the read operation comprising determining if the memory device is being accessed as a dynamic random access memory or as a non-volatile memory in response to a voltage level applied to the word line and, if the memory device is accessed as a non-volatile memory, determining a current difference through the transistor to determine a state of the transistor.

29. (new) The memory device of claim 28 wherein the NROM transistor is coupled to other NROM transistors by a word line coupled to a control gate of each NROM transistor.

30. (new) The memory device of claim 28 wherein the capacitor is coupled between ground and one of either a source or drain region of the NROM transistor.

31. (new) The memory device of claim 29 wherein the NROM transfers data from the capacitor to the data line when the word line is biased at a voltage that is greater than a threshold voltage of the transistor.

32. (new) The memory device of claim 28 wherein a charge stored in the transistor affects a transfer rate of data from the capacitor to the data line.

33. (new) The memory device of claim 29 wherein the capacitor is read when a voltage within a normal operating range of the transistor is applied to the word line.

34. (new) The memory device of claim 33 wherein the voltage is 3.0 volts.